Claims

[c1] What is claimed is:

1.An shallow trench isolation (STI) method for semiconductor processes, the method comprising:

providing a substrate having a top surface;

forming a trench-patterned mask layer on the top surface exposing an unmasked trench region of the substrate, the mask layer comprising a pad oxide layer, and a silicon nitride layer formed on the pad oxide layer;

etching the unmasked region of the substrate to form a trench in the substrate;

depositing a high temperature oxide (HTO) film over the substrate, the HTO film covering the trench and the mask layer;

depositing a dielectric layer that fills the trench and covers the HTO film;

planarizing the dielectric layer to expose the silicon nitride layer; and

stripping the silicon nitride layer;

wherein the HTO film reinforces an interface between the dielectric layer and the substrate to prevent acid penetration and acid-corroded seams forming during the acid solution dipping process.

[c2] 2.The method of claim 1 wherein the HTO film is formed by a low-pressure chemical vapor deposition (LPCVD) process, the LPCVD process utilizing a SiH_2Cl_2/N_2O gas system, a pressure of 0.4 Torr, and a temperature between 700 °C and 850 °C.

[c3] 3.The method of claim 1 wherein the HTO film has a thickness between 50 and 250 angstroms.

[c4] 4.The method of claim 1 wherein the dielectric layer is a high density plasma (HDP) oxide layer.

[c5] 5.The method of claim 1 wherein before stripping the silicon nitride layer, the method further comprises performing a silicon oxide etching process to remove residual silicon oxide from the silicon nitride layer and to simultaneously etch the dielectric layer in the trench.

[c6] 6.The method of claim 1 wherein the acid solution dipping process uses a

diluted HF (DHF) solution.

[c7] 7.The method of claim 1 wherein a 160 ° C phosphoric acid solution is used to strip the silicon nitride layer.